PAGE 4/10 * RCVD AT 5/21/2004 4:08:54 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-34

Serial No.:

10/617,638

Filed:

July 11, 2003

IN THE CLAIMS

Please amend claims 12-25 as follows.

12 (Currently amended) A storage system suitable for storing a plurality of objects each associated with an identification device, said system comprising:

an assembly including a plurality of locations arranged in a row column format, each of the locations adapted to receive an identification device;

row selector logic;

column selector logic;

a two terminal an electronic memory device associated with each identification device, said electronic memory device comprising a first connection, a second connection and an individualized code;

a logic circuit for receiving a serial transmission of the individualized code from an generated between the first connection and the second connection of the electronic memory device at the intersection of a selected row and column;

wherein the transmission is initiated by <u>signals across the first and second</u> connections generated by the row selector circuit and the column selector circuit, which defines the intersection.

13. (Currently amended) A storage system suitable for storing a plurality of objects each associated with an identification device, said system comprising:

an assembly having a plurality of locations each of which are adapted to receive an identification device;

a two terminal an electronic memory device associated with each identification device, each electronic memory device including a <u>first connection</u>, a second connection and a serially transmittable individualized code;

addressing logic; and

PAGE 5/10 * RCVD AT 5/2/1/2004 4:08:54 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-34

Serial No.:

10/617,638

Filed:

July 11, 2003

a logic circuit for receiving serial transmissions <u>originating from the first</u> <u>connection</u> from an addressed <u>identification</u> electronic memory device;

wherein the transmission is transmissions are initiated by signals at the first connection from the addressing logic.

14. (Currently amended) A storage system suitable for storing a plurality of objects each associated with an identification device, said system comprising:

an assembly comprising a plurality of locations each of which are adapted to receive an identification device:

an electronic memory device, associated with each identification device, comprising a data connection, a ground return connection and a serially transmittable individualized code:

logic circuits for signaling the data connection of a selected electronic memory device; and

a logic circuit for receiving the serial transmission of the individualized code from an addressed the data connection of a signaled electronic memory device.

15. (Currently amended) A storage system suitable for storing a plurality of objects each associated with an identification device, said system including an assembly having a plurality of locations each adapted to receive an identification device, said system comprising:

a two terminal electronic memory device, associated with an identification device, that includes a serially transmittable individualized code <u>triggerable and receivable from the two terminals</u>;

addressing logic to initiate transmissions of the individualized code from a selected memory device; and

a processor to receive the serially transmitted individualized code and associate an identification device with a location.

PAGE 6/10 * RCVD AT 5/2/1/2004 4:08:54 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-34

Serial No.:

10/617,638

Filed:

July 11, 2003

16. (Currently amended) A storage system suitable for storing a plurality of objects each associated with an identification device, said system comprising:

a plurality of mechanically coupled locations, each adapted to receive an identification device;

an electronic memory device, associated with each identification device, comprising a data connection and a ground return connection and a scrially transmittable individualized code;

addressing logic;

a processor;

wherein the addressing logic signals a memory device via its data and ground return connections to transmit its individualized code and wherein the processor receives an individualized code originating from the data and ground connections and associates the individualized code with a location.

17. (Currently amended) A storage system suitable for storing a plurality of objects each associated with an identification device, a plurality of mechanically coupled locations adapted to receive an identification device, said system comprising:

an electronic memory device, associated with each identification device, comprising a data connection, a ground return connection and a serially transmittable individualized code;

addressing logic;

processing logic;

wherein the addressing logic signals a memory device via its data and ground return connections to transmit its individualized code, and wherein the processing logic associates the individualized code with a location after receiving the code from the signaled data connection.

18. (Currently amended) A storage system suitable for storing a plurality of objects each associated with an identification device, said system including an assembly having a plurality of locations each adapted to receive an identification device, said system comprising:

PACE 7/10 * RCVD AT 5/2/1/2004 4:08:54 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID: * DURATION (mm-ss):02-34

Serial No.:

10/617,638

Filed:

July 11, 2003

a two terminal electronic device associated with an identification device for transmitting an individualized code;

addressing logic to initiate transmissions from the two terminals of the electronic device; and

a processor to receive a transmitted individualized code from the two terminals and associate the identification device with a location.

- 19. (Previously presented) The system as claimed in claim 12, wherein the individualized code comprises a plurality of bits.
- 20. (Previously presented) The system as claimed in claim 13, wherein the individualized code comprises a plurality of bits.
- 21. (Previously presented) The system as claimed in claim 14, wherein the individualized code comprises a plurality of bits.
- 22. (Previously presented) The system as claimed in claim 15, wherein the individualized code comprises a plurality of bits.
- 23. (Previously presented) The system as claimed in claim 16, wherein the individualized code comprises a plurality of bits.
- 24. (Previously presented) The system as claimed in claim 17, wherein the individualized code comprises a plurality of bits.
- 25. (Previously presented) The system as claimed in claim 18, wherein the individualized code is scrially transmittable and comprises a plurality of bits.